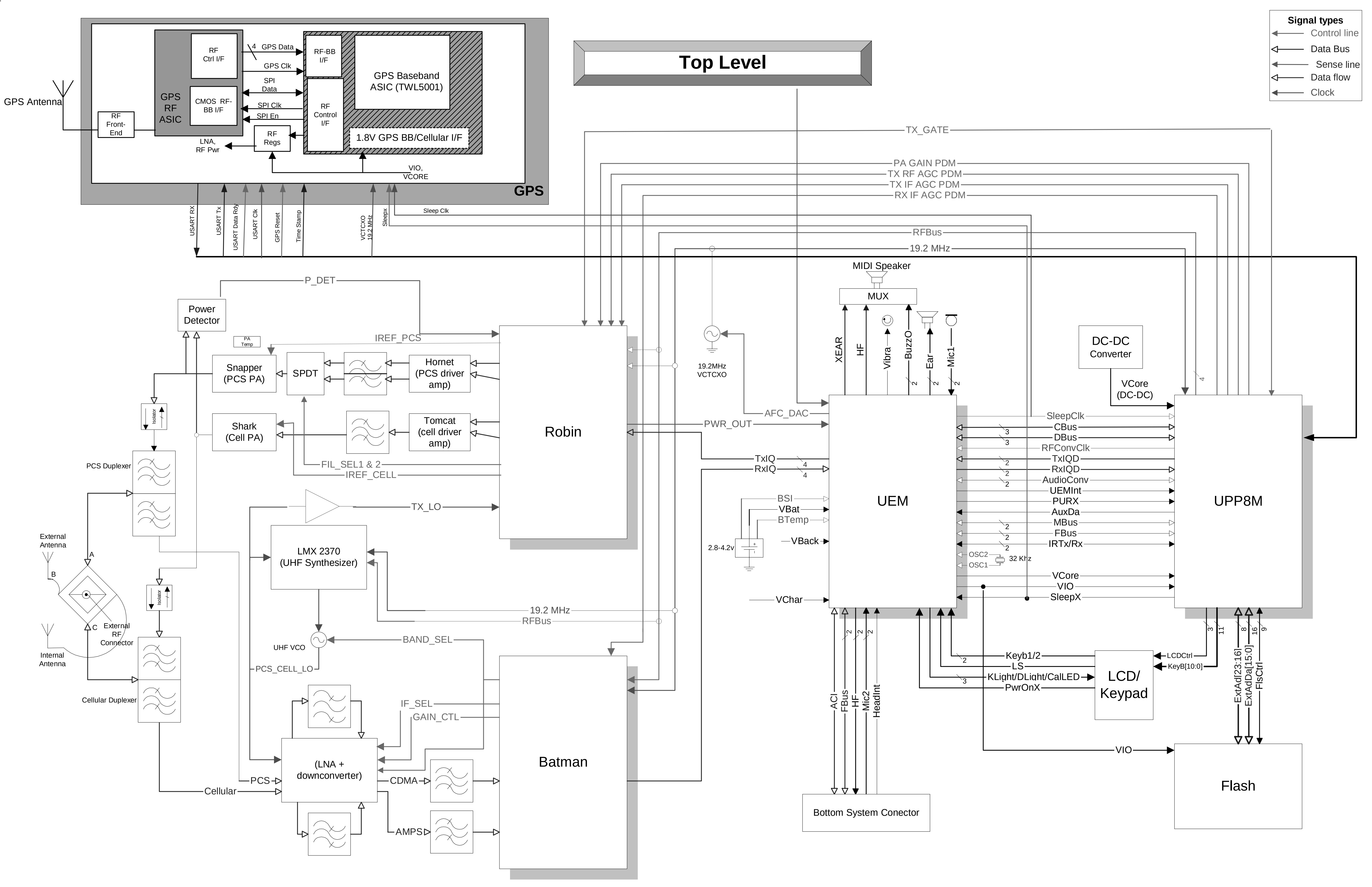
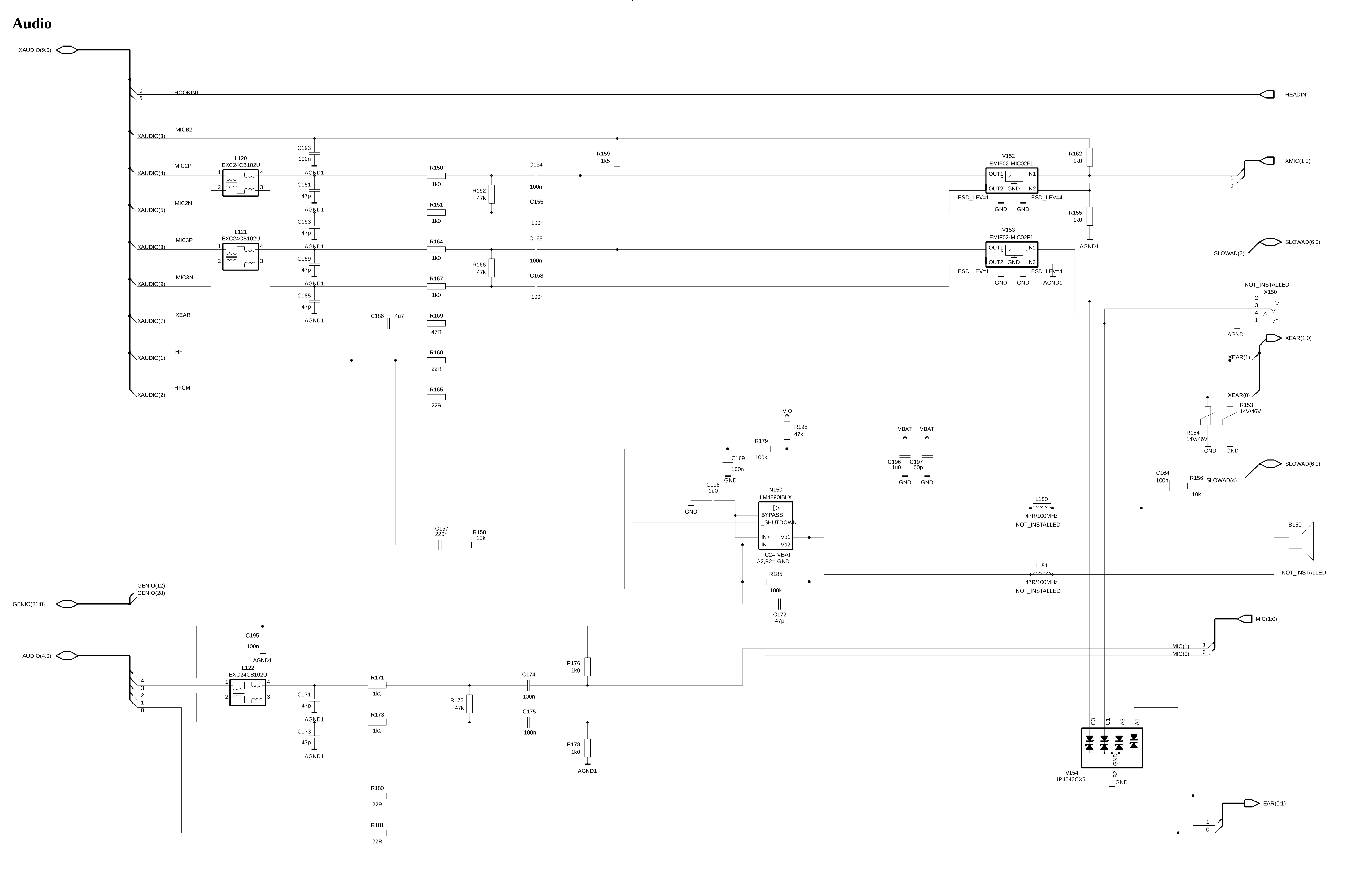
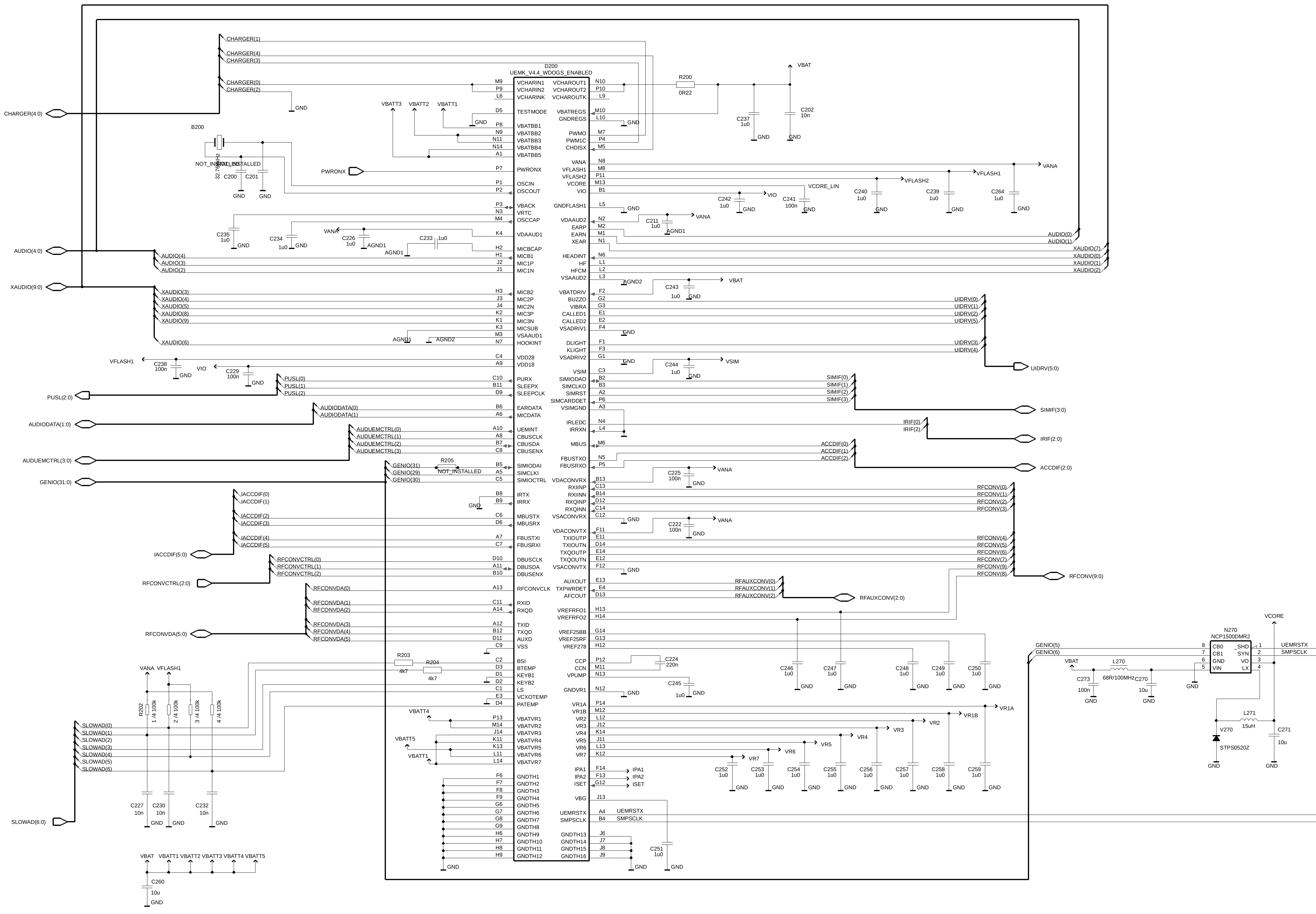
3585i Top Level Overview



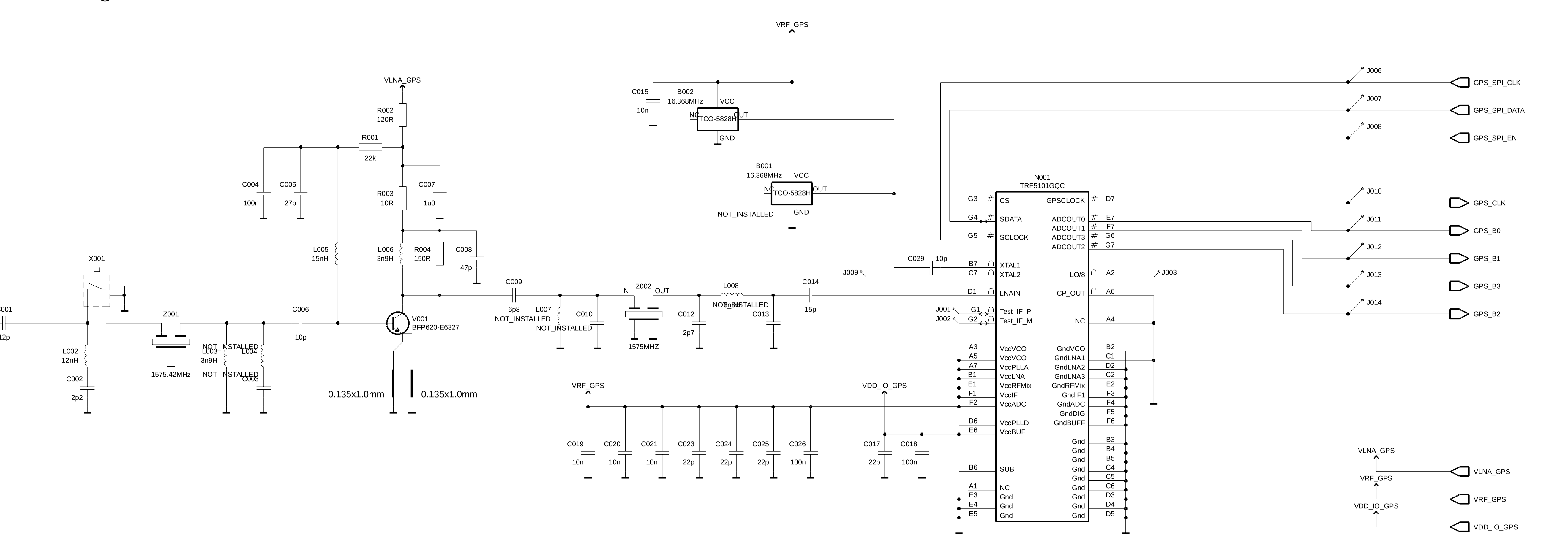
Audio


XAUDIO(9:0)
HOOKINT
HEADINT
MICB2
XAUDIO(3)
MIC2P
XAUDIO(4)
MIC2N
XAUDIO(5)
MIC3P
XAUDIO(8)
MIC3N
XAUDIO(9)
XEAR
XAUDIO(7)
HF
XAUDIO(1)
HFCM
XAUDIO(2)
L120 EXC24CB102U
L121 EXC24CB102U
L122 EXC24CB102U
C193 100n
C151 47p
C153 47p
C159 47p
C185 47p
AGND1
R150 1k0
R151 1k0
R164 1k0
R167 1k0
R152 47k
R166 47k
C154 100n
C155 100n
C165 100n
C168 100n
C186 4u7
R169 47R
R160 22R
R165 22R
R159 1k5
R162 1k0
R155 1k0
V152 EMIF02-MIC02F1
V153 EMIF02-MIC02F1
OUT1 IN1 OUT2 GND IN2
ESD_LEV=1
ESD_LEV=4
GND
XMIC(1:0)
SLOWAD(6:0)
SLOWAD(2)
NOT_INSTALLED
X150
XEAR(1:0)
XEAR(1)
XEAR(0)
R153 14V/46V
R154 14V/46V
VIO
R195 47k
R179 100k
C169 100n
C198 1u0
VBAT
C196 1u0
C197 100p
N150 LM4890IBLX
BYPASS
_SHUTDOWN
IN+ IN- Vo1 Vo2
C2= VBAT
A2,B2= GND
R185 100k
C172 47p
C157 220n
R158 10k
C164 100n
R156 10k
SLOWAD(4)
L150 47R/100MHz NOT_INSTALLED
L151 47R/100MHz NOT_INSTALLED
B150
GENIO(12)
GENIO(28)
GENIO(31:0)
AUDIO(4:0)
C195 100n
R176 1k0
R178 1k0
C171 47p
C173 47p
R171 1k0
R173 1k0
R172 47k
C174 100n
C175 100n
MIC(1:0)
MIC(1)
MIC(0)
V154 IP4043CX5
C3 C1 A3 A1 B2
R180 22R
R181 22R
EAR(0:1)

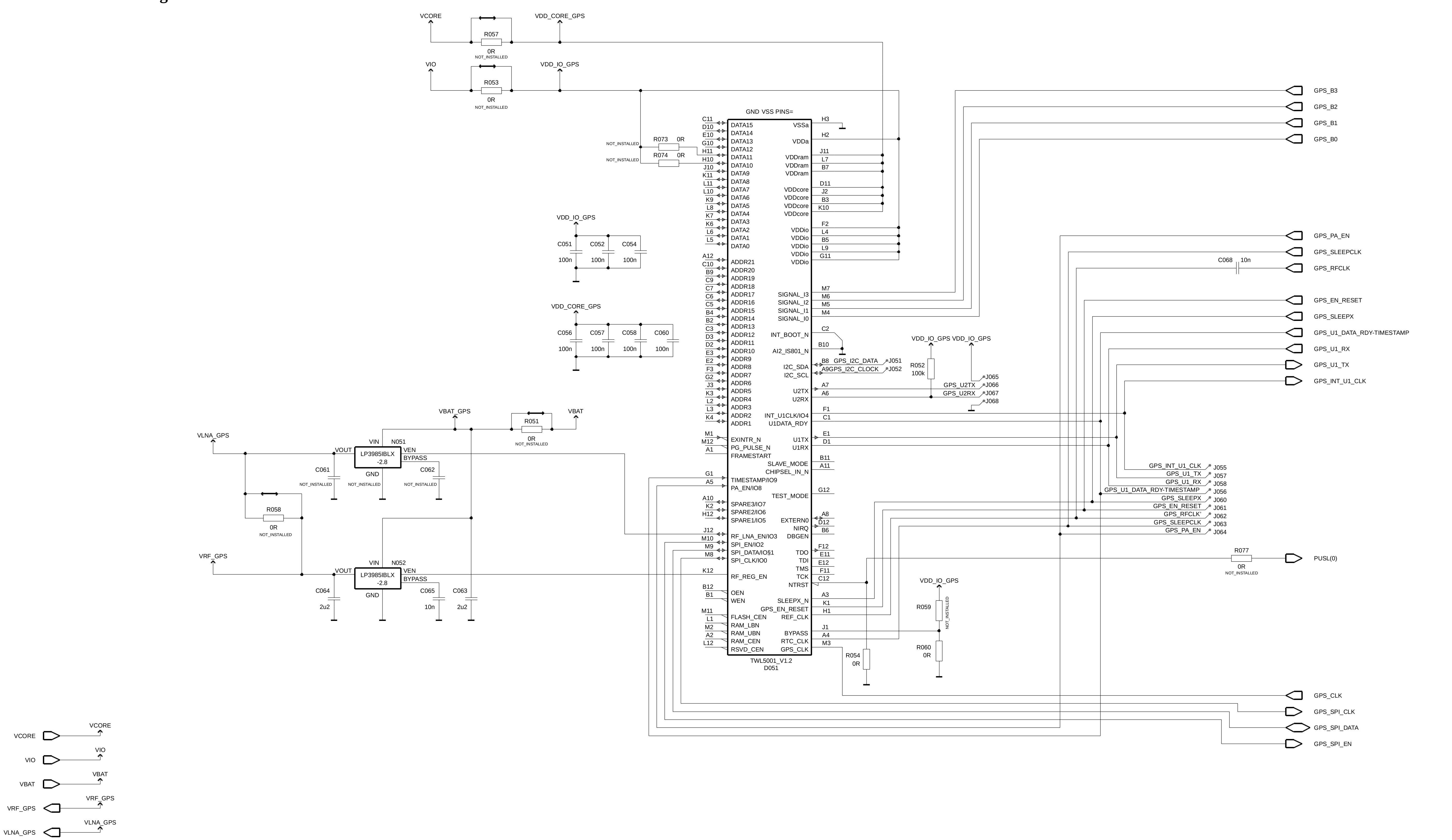
DCT4 Common Baseband



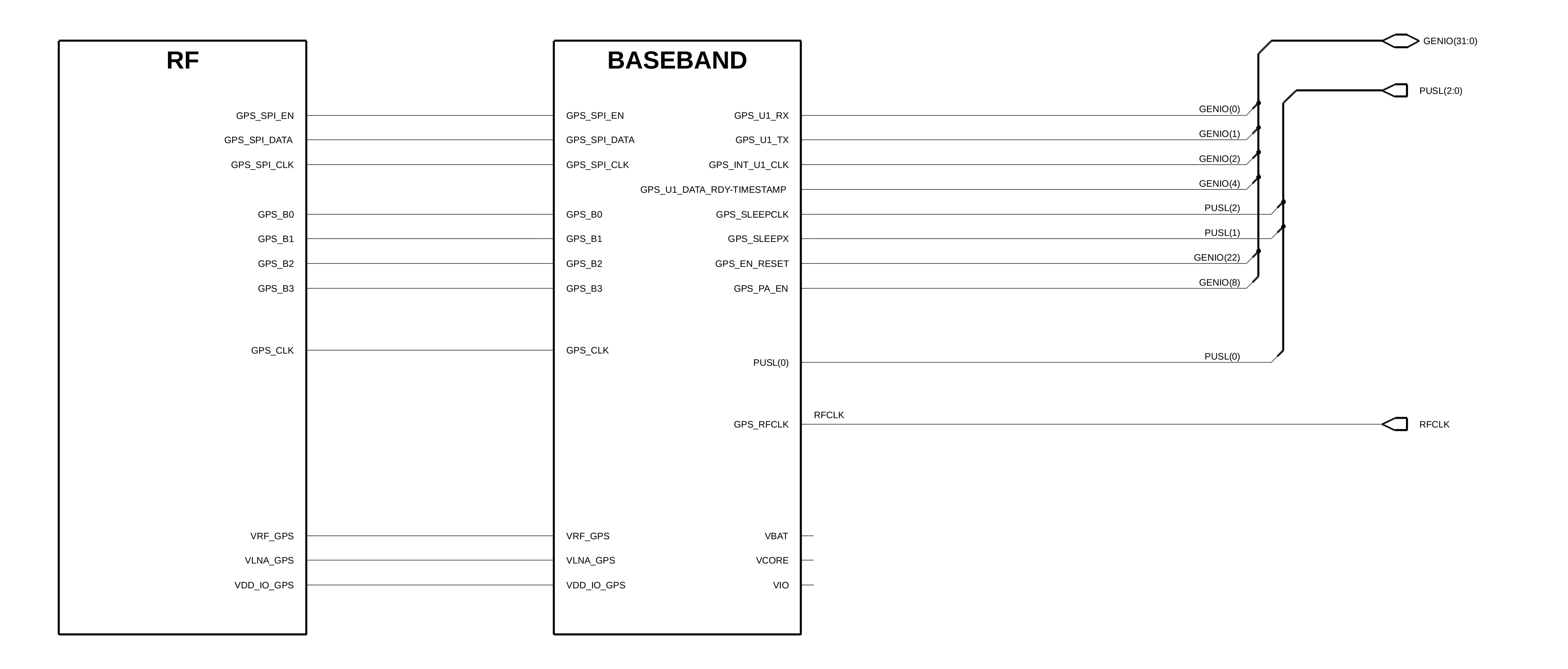
GPS RF Circuit Diagram



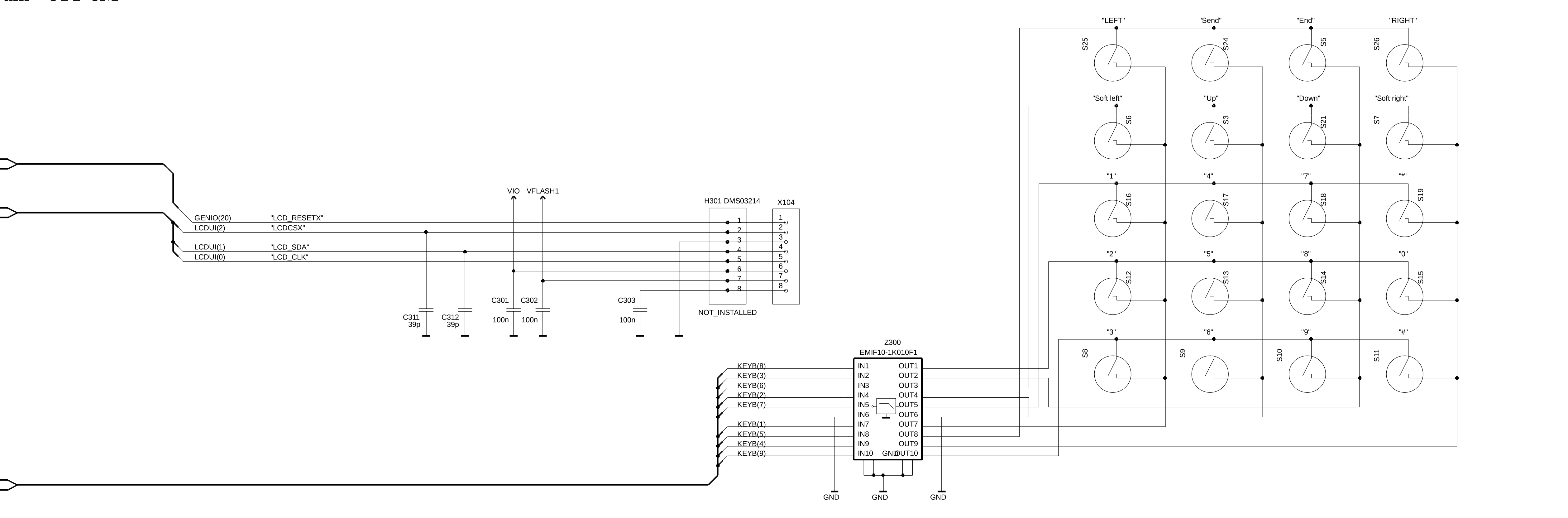
GPS Baseband Circuit Diagram

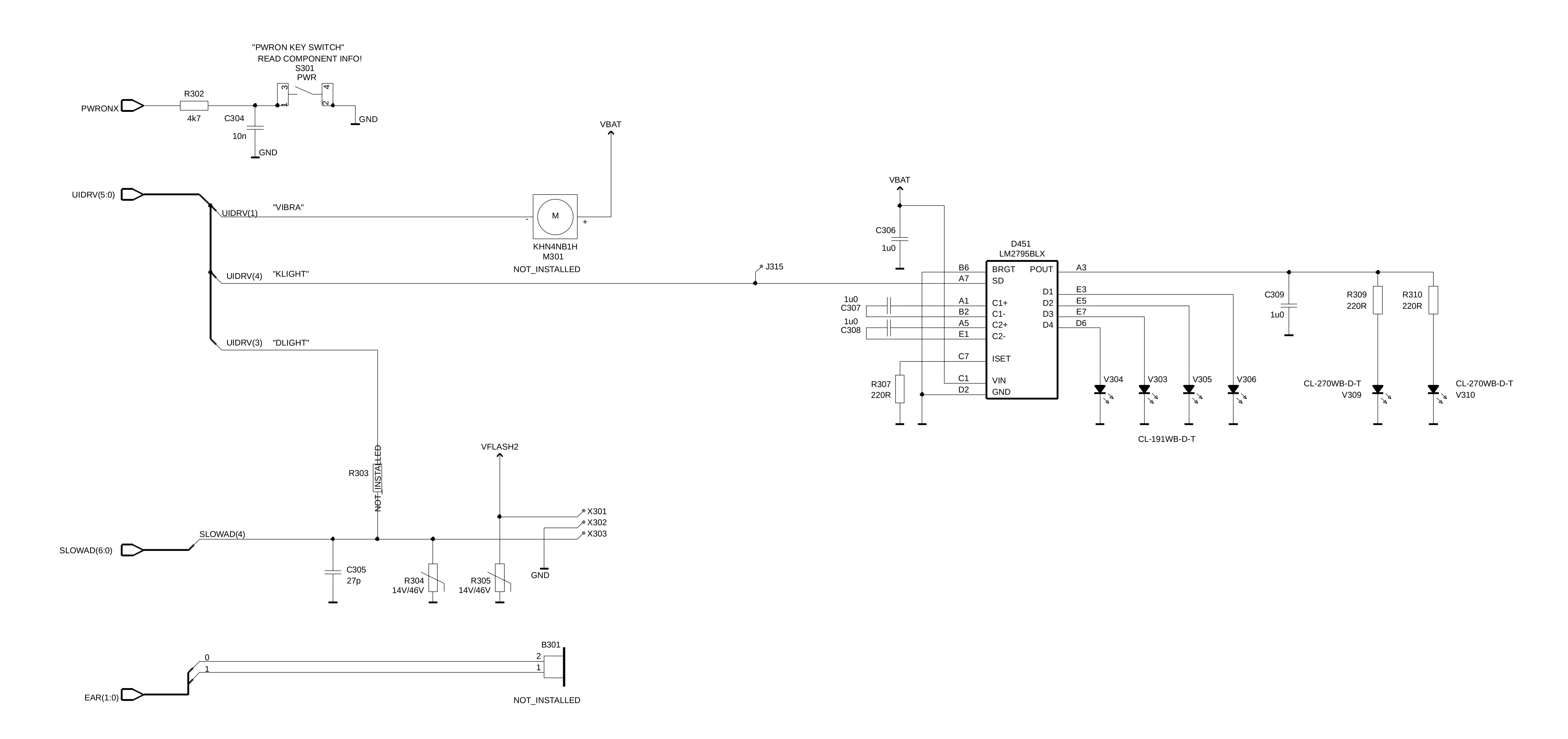


GPS RF-BB Interface

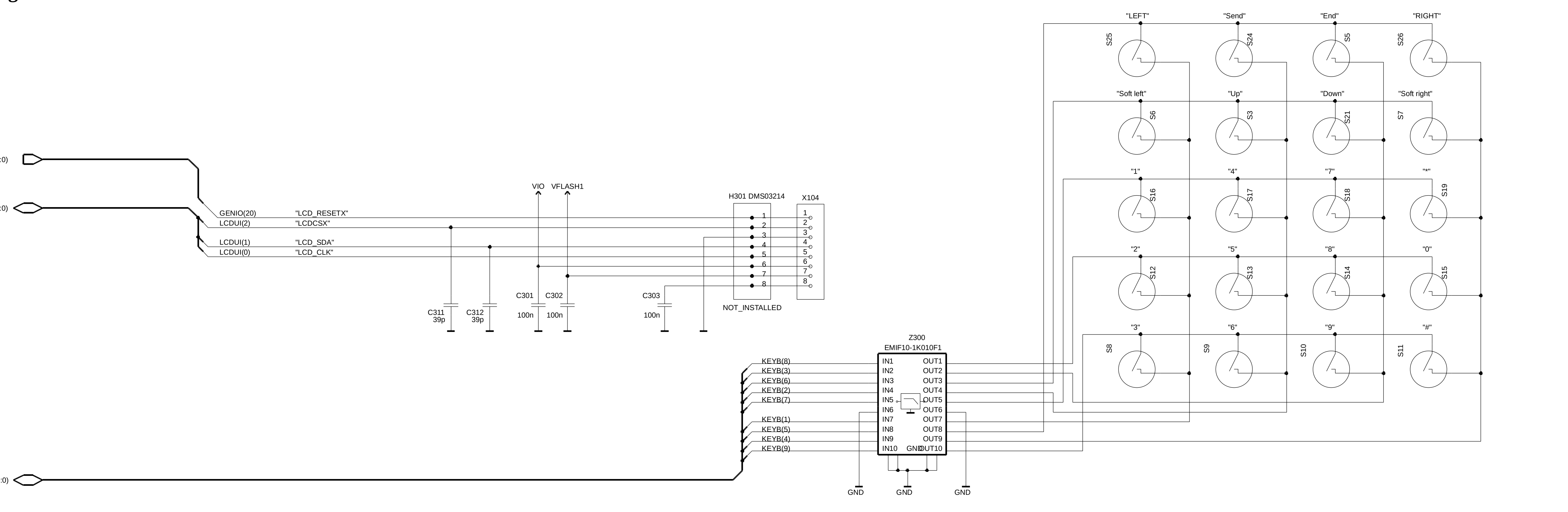
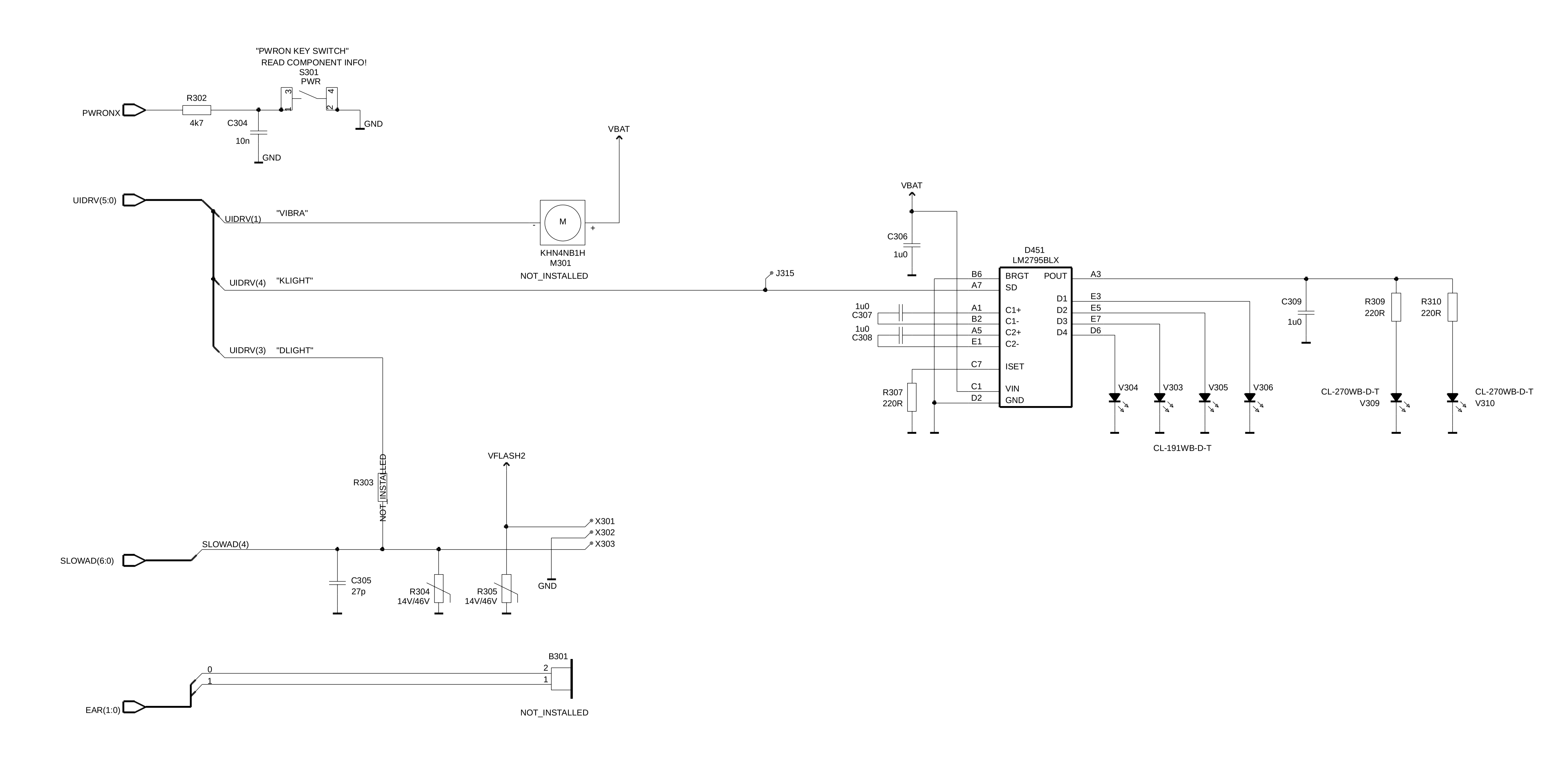


Circuit Diagram - UPP 8M





Circuit Diagram - User Interface

BB-RF Interface

GENIO(31:0)
13 --> FAST_AGC
03 --> PA_IS2000
25 --> SYNTH_LE
09 --> RX_IF_AGC
26 --> TX_RF_AGC
07 --> TX_IF_AGC
11 --> PA_GAIN
08 --> TX_GATE

R435 4k7
C428 10n GND
C435 10n GND
R433 1k0
R434 4k7
C426 10n GND
C427 1n0 GND
C429 33n
V420 DTC143ZETL IN OUT R1 4k7 R2 47k MODEL GND
R427 1k0
R428 4k7
C422 10n GND
C423 1n0 GND
C430 33n
V421 DTC143ZETL IN OUT R1 4k7 R2 47k MODEL GND
R430 1k0
R431 4k7
C424 10n GND
C425 1n0 GND
C431 33n
V422 DTC143ZETL IN OUT R1 4k7 R2 47k MODEL GND

GENIO_O(31:0): 09, 26, 07, 11, 03, 25, 08, 12, 13

RFCONV(9:0) — RFCONV_O(9:0)
8 --> VREFRF02 8
9 --> VREFRF01 9
0 <-- RX_IP 0
1 <-- RX_IN 1
2 <-- RX_QP 2
3 <-- RX_QN 3
4 --> TX_IP 4
5 --> TX_IN 5
6 --> TX_QP 6
7 --> TX_QN 7

RFAUXCONV(2:0) — RFAUXCONV_O(2:0)
0 --> AUXOUT 0
1 <-- PWROUT 1
2 --> AFC 2

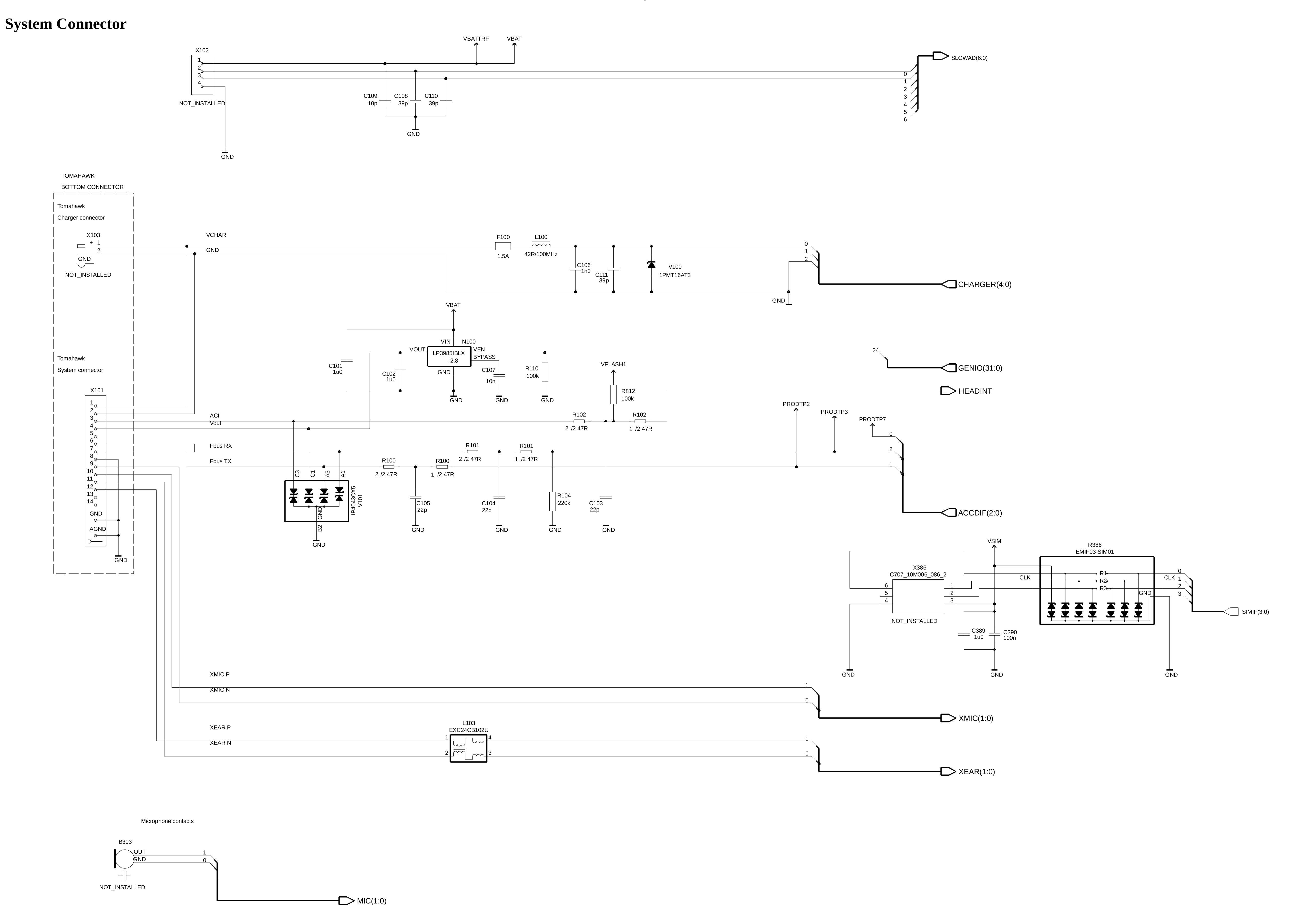
RFCLK <-- 19.2_MHZ RFCLK_I
RFCLKGND <-- 19.2_MHZGND RFCLKGND_I

PUSL(2:0) — PUSL_O(2:0)
0 --> PURX 0
1 --> SLEEPX 1
2 --> SLEEPCLK 2

SLOWAD(6:0) — SLOWAD_O(6:0)
3 <-- FALSE_DET 3
6 <-- PA_TEMP 6

RFICCNTRL(2:0) — RFICCNTRL_O(2:0)
0 --> RFBusClk 0
1 <-> RFBusData 1
2 --> RFBusEn1X 2

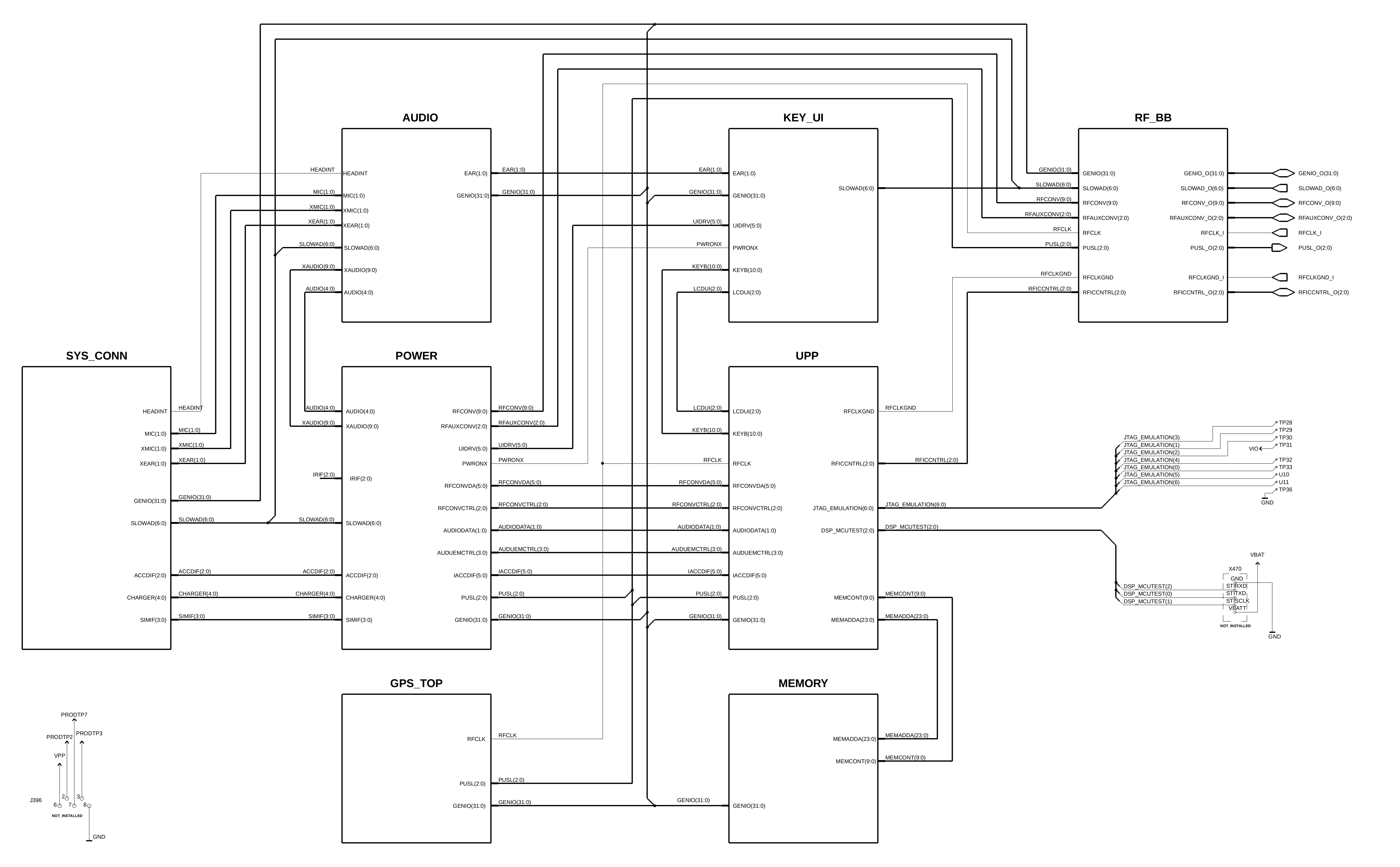
System Connector



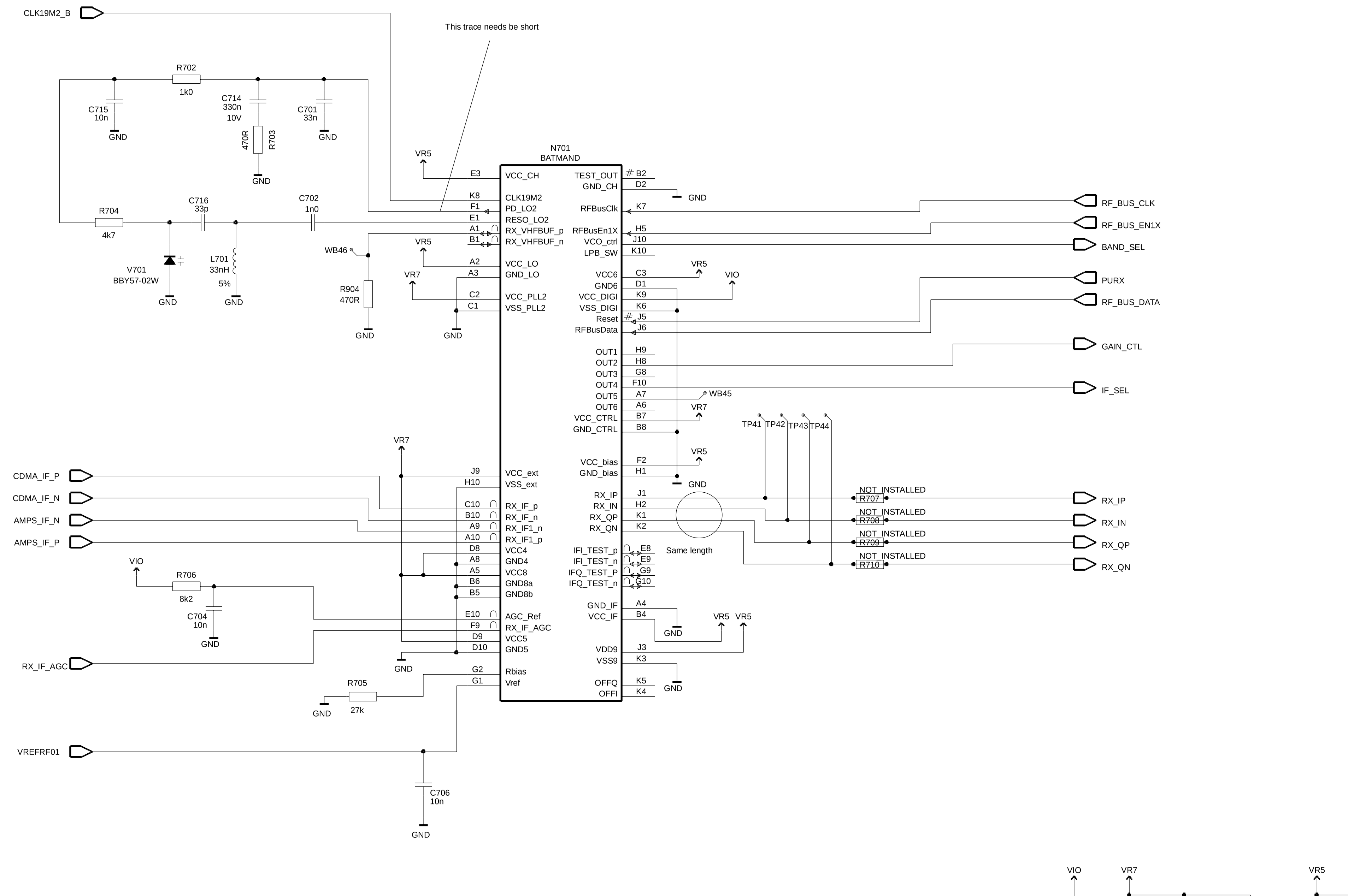
AMD 64 Mbit

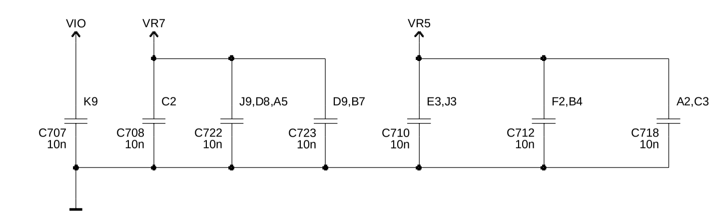
GENIO(31:0)
MEMADDA(23:0)
MEMCONT(9:0)
D450
AM29N643GT70MVAI
FLASHM 4Mx16
A 0 4194303
NC
CLK
_AVD
_CE
_RESET
_OE
_WE
_WP
RDY
PS
ADDRESS/DATA I/O
B2 A9 B8 A8 B3 A2 A10 A4 B4 B9 B6 C10 A6 B7 A1 B5
D10 D9 C7 C6 D5 D4 C3 C2 C9 C8 D7 D6 C5 C4 D2 D1
NC 1 NC 2 NC 3 NC 4 NC 5 NC 6 NC 7 NC 8
A5= VIO
B1,D8= VIO
A7= VPP
A3,C1,B10,D3= GND
R450
4k7
VPP
VPP VIO VIO
C454 10n
C450 10n
C451 100n
GND GND GND

DCT4 Common Baseband - Top Level

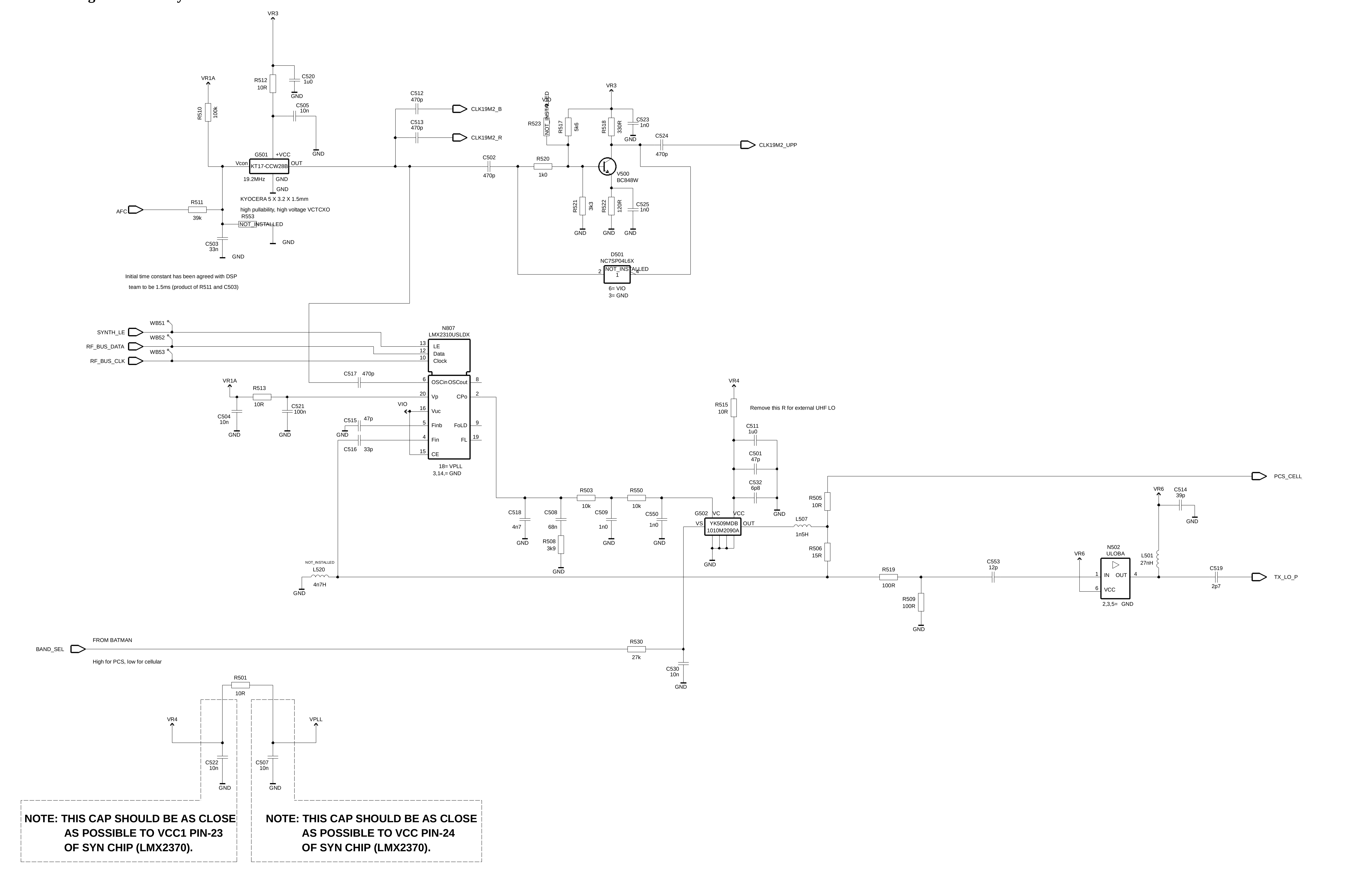


Circuit Diagram - Batman

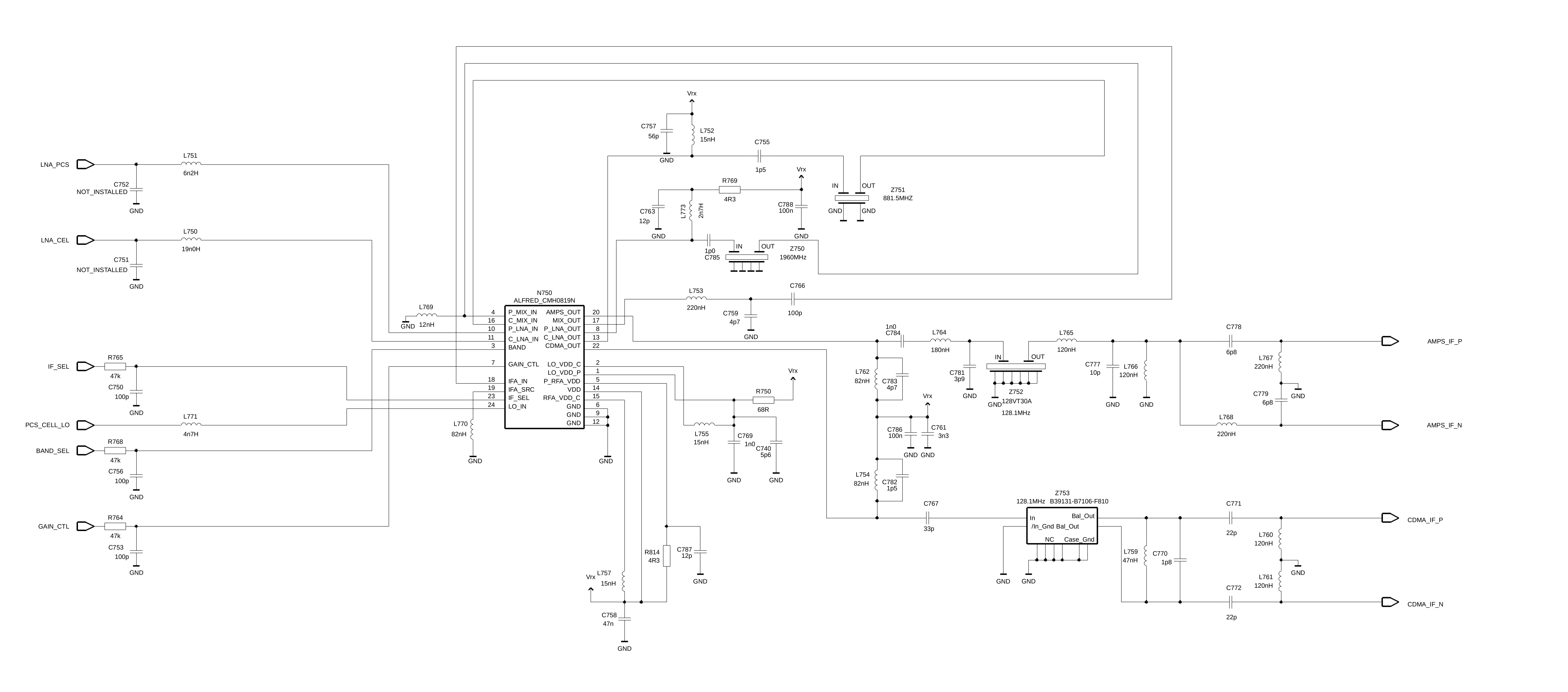




Circuit Diagram - UHF Synth

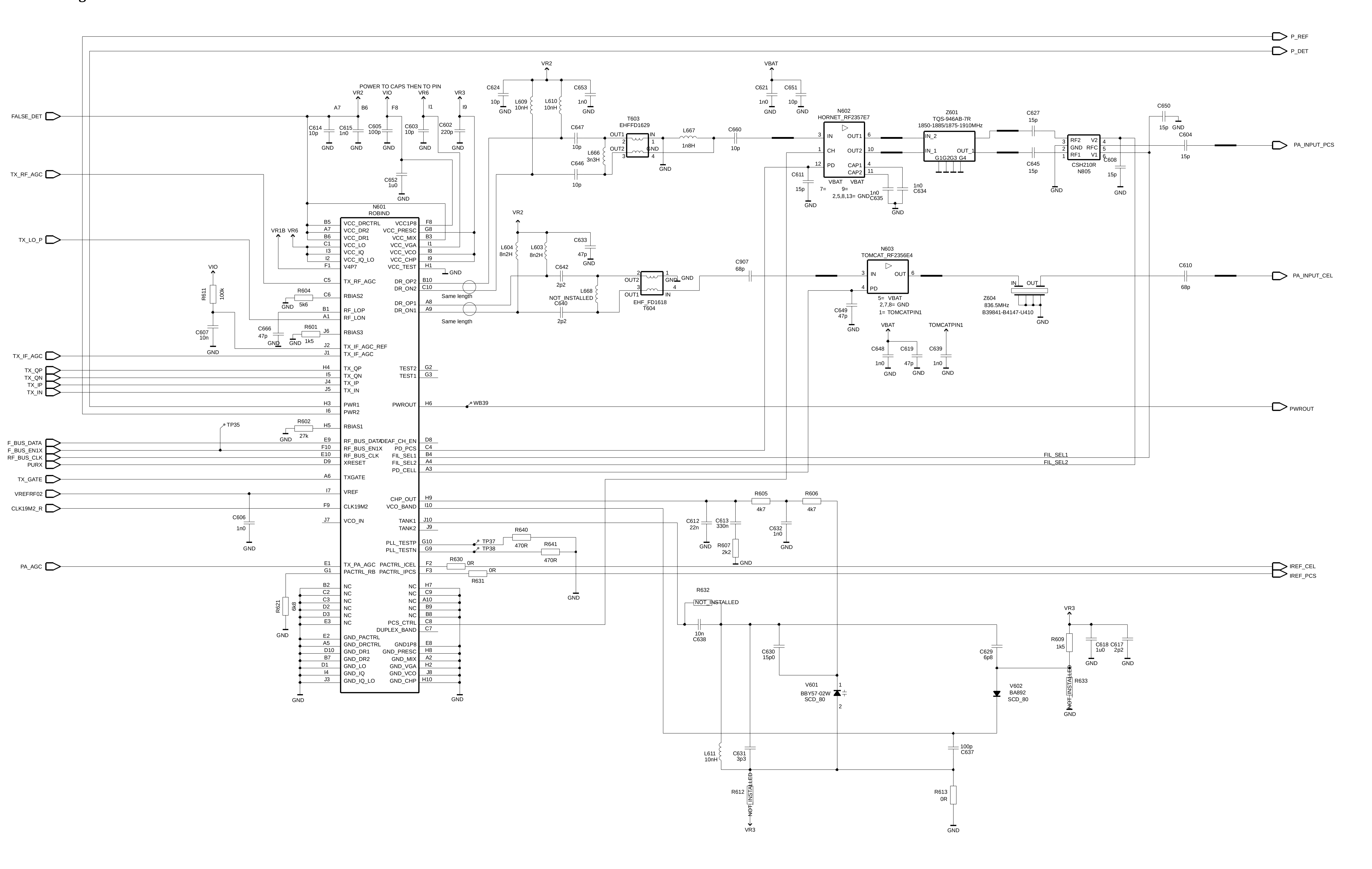


Circuit Diagram - Front End

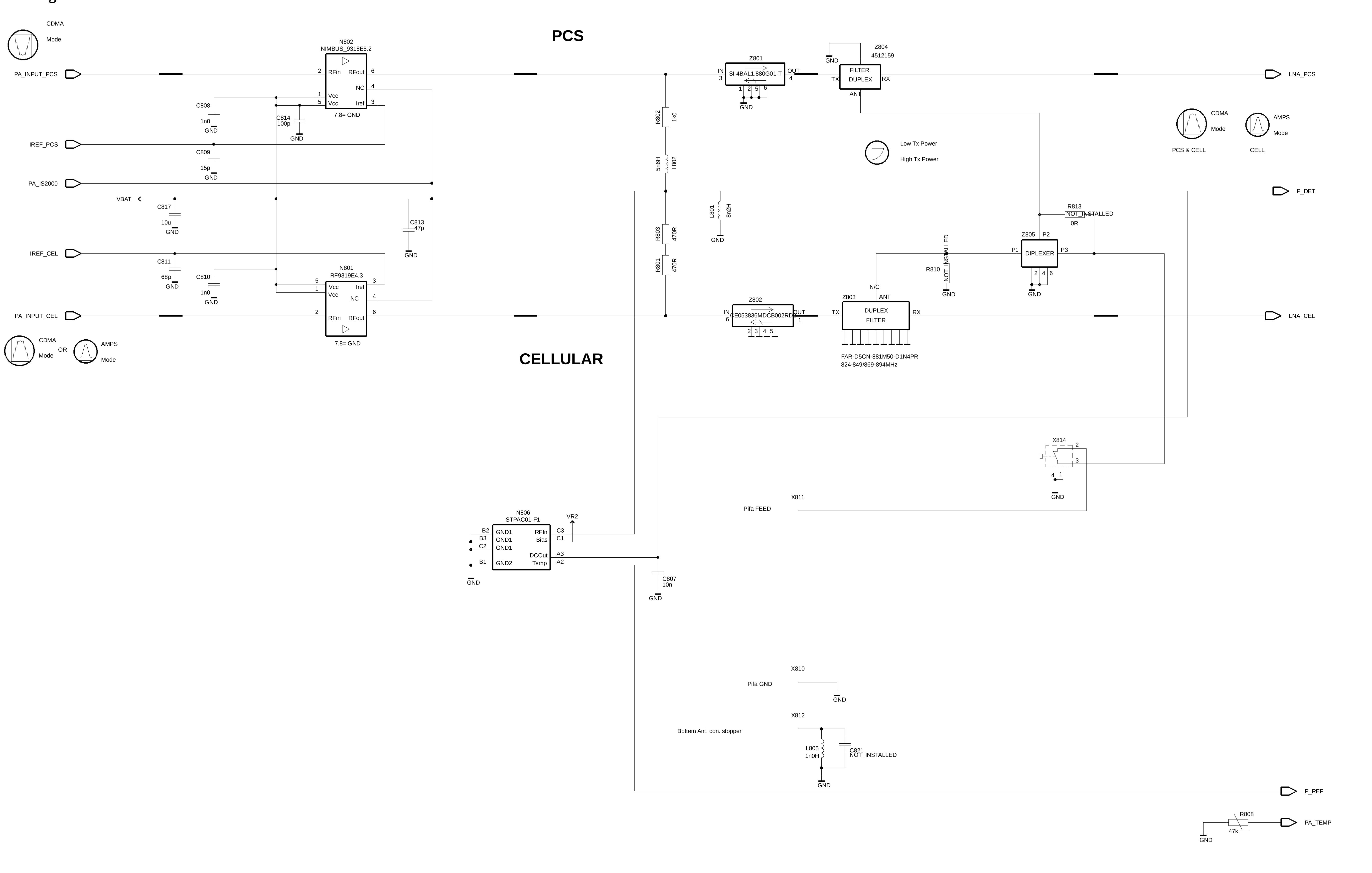


MODES	LOGIC INPUTS		
	BAND	GAIN_CTL	IF_SEL
CEL CDMA Hi Gain	0	1	0
CEL CDMA Lo Gain	0	0	0
PCS CDMA Hi Gain	1	1	0
PCS CDMA Lo Gain	1	0	0
AMPS Hi Gain	0	1	1
AMPS Lo Gain	0	0	1

Circuit Diagram - Robin

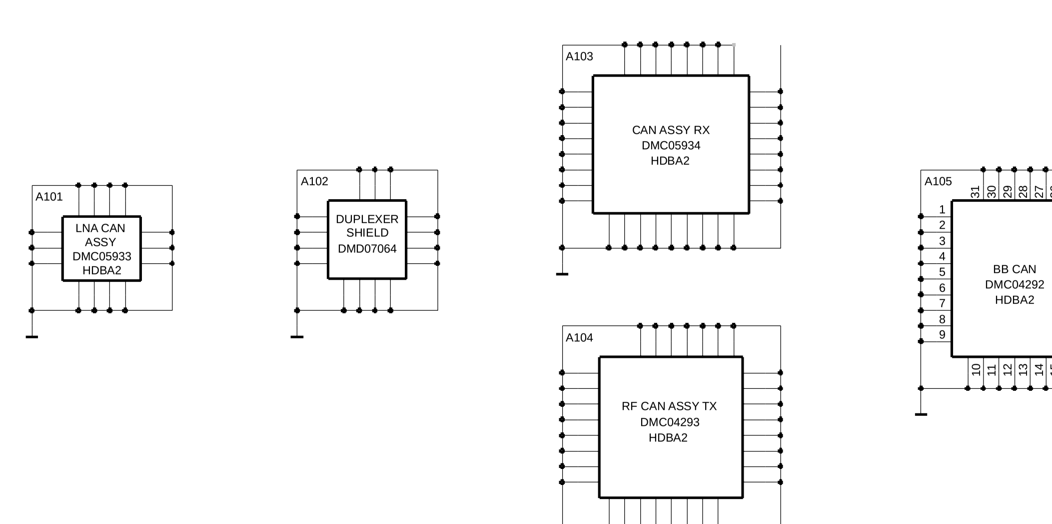


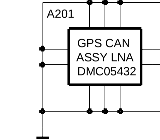
Circuit Diagram - PA



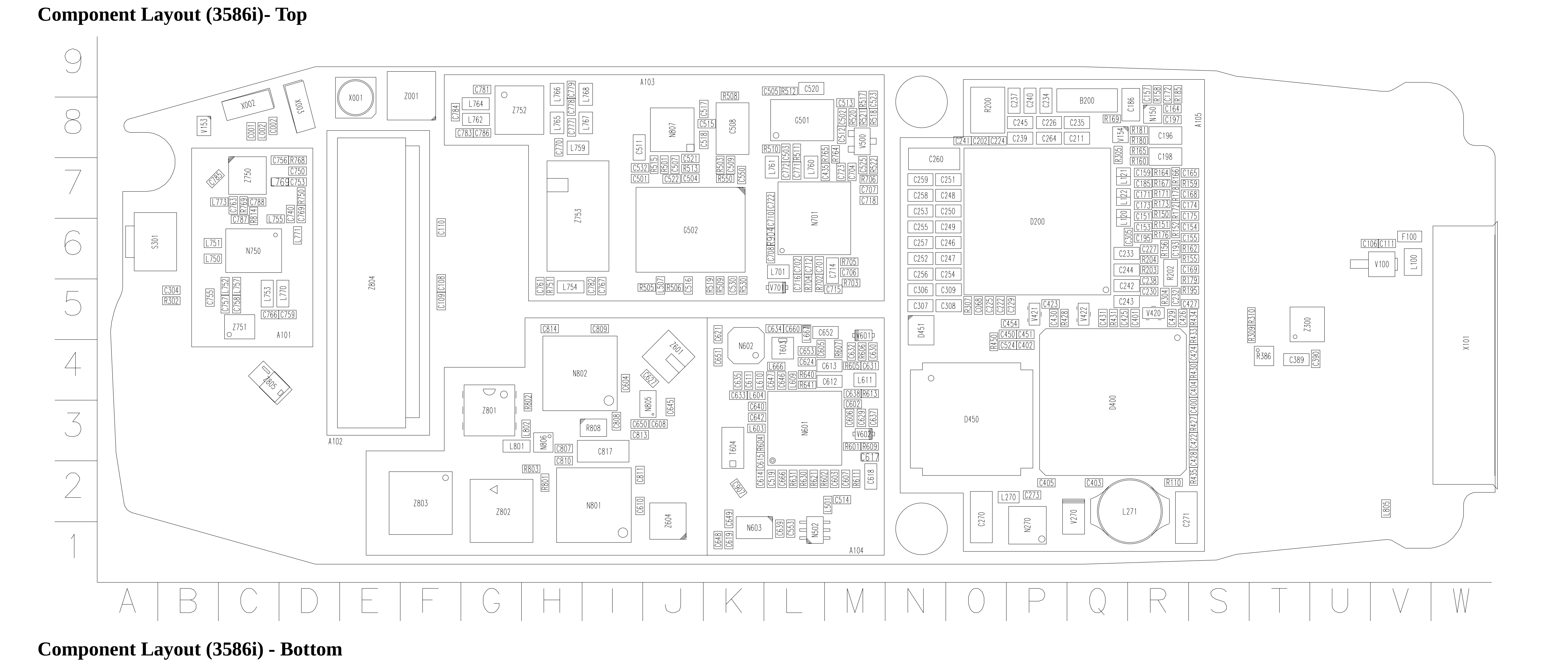
Circuit Diagram - Top Levell

Shields


A101
LNA CAN
ASSY
DMC05933
HDBA2
A102
DUPLEXER
SHIELD
DMD07064
A103
CAN ASSY RX
DMC05934
HDBA2
A104
RF CAN ASSY TX
DMC04293
HDBA2
A105
BB CAN
DMC04292
HDBA2


A201
GPS CAN
ASSY LNA
DMC05432

Component Layout (3586i)- Top



Component Layout (3586i) - Bottom